Release 14.2 - xst P.28xd (nt64)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs

Total CPU time to Xst completion: 1.03 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs

Total CPU time to Xst completion: 1.03 secs

--> Reading design: UART\_top\_hw\_test.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "UART\_top\_hw\_test.prj"

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "UART\_top\_hw\_test"

Output Format : NGC

Target Device : xc6slx16-2-csg324

---- Source Options

Top Module Name : UART\_top\_hw\_test

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 16

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : Yes

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

---- Other Options

Cores Search Directories : {"ipcore\_dir" }

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\* HDL Parsing \*

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Parsing VHDL file "C:\Users\SAYO\Desktop\UART\parity\_calculation.vhd" into library work

Parsing package <parity\_calculation>.

Parsing package body <parity\_calculation>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\UART\_error\_generation.vhd" into library work

Parsing entity <UART\_error\_generation>.

Parsing architecture <UART\_error\_generation\_arch> of entity <uart\_error\_generation>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\transmit\_state\_machine.vhd" into library work

Parsing entity <transmit\_state\_machine>.

Parsing architecture <transmit\_state\_machine\_arch> of entity <transmit\_state\_machine>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\transmit\_shift\_register.vhd" into library work

Parsing entity <transmit\_shift\_register>.

Parsing architecture <transmit\_shift\_register\_arch> of entity <transmit\_shift\_register>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\receive\_state\_machine.vhd" into library work

Parsing entity <receive\_state\_machine>.

Parsing architecture <receive\_state\_machine\_arch> of entity <receive\_state\_machine>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\receive\_signal\_synchronizer.vhd" into library work

Parsing entity <receive\_signal\_synchronizer>.

Parsing architecture <receive\_signal\_synchronizer\_arch> of entity <receive\_signal\_synchronizer>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\receive\_shift\_register.vhd" into library work

Parsing entity <receive\_shift\_register>.

Parsing architecture <receive\_shift\_register\_arch> of entity <receive\_shift\_register>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" into library work

Parsing entity <FIFO>.

Parsing architecture <FIFO\_a> of entity <fifo>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" into library work

Parsing entity <UART\_top>.

Parsing architecture <UART\_top\_arch> of entity <uart\_top>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\ipcore\_dir\uart\_clk\_gen.vhd" into library work

Parsing entity <uart\_clk\_gen>.

Parsing architecture <xilinx> of entity <uart\_clk\_gen>.

Parsing VHDL file "C:\Users\SAYO\Desktop\UART\UART\_top\_hw\_test.vhd" into library work

Parsing entity <UART\_top\_hw\_test>.

Parsing architecture <UART\_top\_hw\_test\_arch> of entity <uart\_top\_hw\_test>.

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\* HDL Elaboration \*

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Elaborating entity <UART\_top\_hw\_test> (architecture <UART\_top\_hw\_test\_arch>) with generics from library <work>.

Elaborating entity <uart\_clk\_gen> (architecture <xilinx>) from library <work>.

Elaborating entity <UART\_top> (architecture <UART\_top\_arch>) with generics from library <work>.

Elaborating entity <receive\_signal\_synchronizer> (architecture <receive\_signal\_synchronizer\_arch>) from library <work>.

Elaborating entity <receive\_state\_machine> (architecture <receive\_state\_machine\_arch>) with generics from library <work>.

INFO:HDLCompiler:679 - "C:\Users\SAYO\Desktop\UART\receive\_state\_machine.vhd" Line 260. Case statement is complete. others clause is never selected

Elaborating entity <receive\_shift\_register> (architecture <receive\_shift\_register\_arch>) with generics from library <work>.

WARNING:HDLCompiler:746 - "C:\Users\SAYO\Desktop\UART\receive\_shift\_register.vhd" Line 51: Range is empty (null range)

WARNING:HDLCompiler:220 - "C:\Users\SAYO\Desktop\UART\receive\_shift\_register.vhd" Line 51: Assignment ignored

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 114: Formal port <rst> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 115: Formal port <wr\_clk> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 116: Formal port <rd\_clk> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 117: Formal port <din> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 118: Formal port <wr\_en> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 119: Formal port <rd\_en> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 120: Formal port <dout> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 121: Formal port <full> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 122: Formal port <almost\_full> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 123: Formal port <empty> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

ERROR:HDLCompiler:1156 - "C:\Users\SAYO\Desktop\UART\receive\_top.vhd" Line 124: Formal port <almost\_empty> does not exist in entity <FIFO>. Please compare the definition of block <FIFO> to its component declaration and its instantion to detect the mismatch.

INFO:HDLCompiler:1408 - "C:\Users\SAYO\Desktop\UART\ipcore\_dir\FIFO.vhd" Line 43. fifo is declared here

Elaborating entity <FIFO> (architecture <FIFO\_a>) from library <work>.

Execution of entity fifo failed

Netlist UART\_top(32,8,true,true,2,64,8,8)(UART\_top\_arch) remains a blackbox, due to errors in its contents

-->

Total memory usage is 218816 kilobytes

Number of errors : 11 ( 0 filtered)

Number of warnings : 2 ( 0 filtered)

Number of infos : 0 ( 0 filtered)